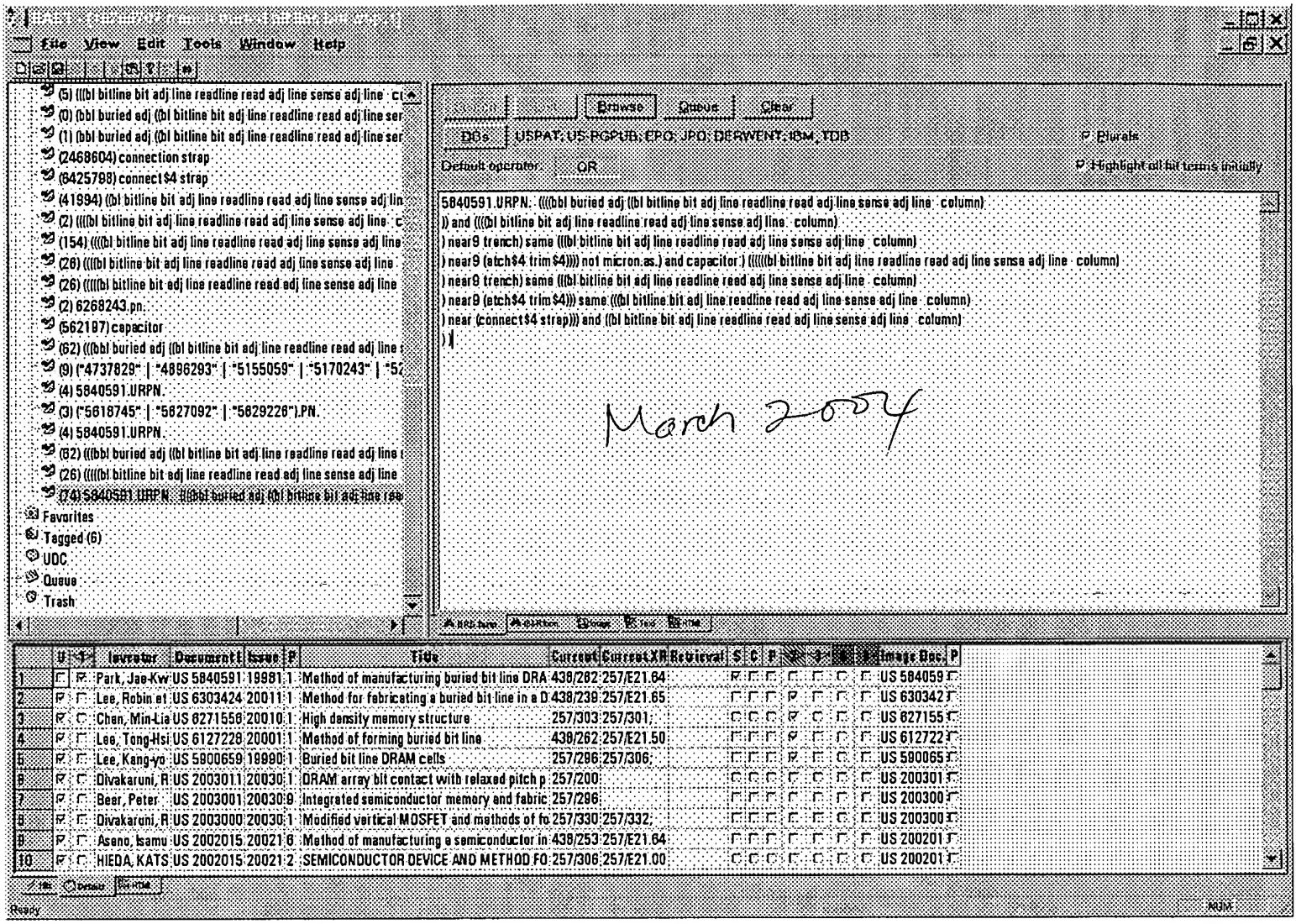

	U	S	Inventor	Document	Issue	P	Title	Current	Current XR	Retrieval	S	C	P					Image Doc.	P
1		☑	Park, Jae-Kw	US 5840591	19981	1	Method of manufacturing buried bit line DRA	438/262	257/E21.64		☑							US 584059	
2	☑		Lee, Robin et	US 6303424	20011	1	Method for febricating a buried bit line in a D	438/239	257/E21.65					☑				US 630342	
3	☑		Chen, Min-Lia	US 6271556	20010	1	High density memory structure	257/303	257/301;					☑				US 627155	
4	☑		Lee, Tong-Hsi	US 6127228	20001	1	Method of forming buried bit line	438/262	257/E21.50					☑				US 612722	
5	☑		Lee, Kang-yo	US 5800659	19980	1	Buried bit line DRAM cells	257/296	257/306;					☑				US 580065	
6	☑		Divakaruni, R	US 2003011	20030	1	DRAM array bit contact with relaxed pitch p	257/200										US 200301	
7	☑		Beer, Peter	US 2003001	20030	9	Integrated semiconductor memory and fabric	257/296										US 200300	
8	☑		Divakaruni, R	US 2003000	20030	1	Modified vertical MOSFET and methods of fo	257/330	257/332;									US 200300	
9	☑		Aseno, Isamu	US 2002015	20021	6	Method of manufacturing a semiconductor in	438/253	257/E21.64									US 200201	
10	☑		HIEDA, KATS	US 2002015	20021	2	SEMICONDUCTOR DEVICE AND METHOD FO	257/306	257/E21.00									US 200201	

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